WHAT IS CLAIMED IS:

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1. A semiconductor device, comprising:

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region;

at least one of a source/drain region formed above the isolation region.

2. The semiconductor device as recited in Claim 1 wherein the isolation region is formed adjacent the semiconductor substrate.

3. The semiconductor device as recited in Claim 1 wherein the isolation region is not located under a channel region.

4. The semiconductor device as recited in Claim 1 wherein the isolation region comprises an oxide.

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5. The semiconductor device as recited in Claim 1 wherein a portion of the at least one source/drain region comprises polysilicon.

6. The semiconductor device as recited in Claim 1 wherein the isolation region extends through a transistor tub.

7. A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation region located in the trench; and

a source/drain region located over the isolation region.

8. The semiconductor device as recited in Claim 7 wherein the isolation region is not located under the channel region.

9. The semiconductor device as recited in Claim 7 wherein the isolation region comprises an oxide.

10. The semiconductor device as recited in Claim 7 wherein the source/drain region includes a first portion located in the semiconductor substrate and a second portion comprising polysilicon located on the isolation region.

11. The semiconductor device as recited in Claim 7 wherein the isolation region extends through a transistor tub.

12. A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

an isolation region located adjacent the channel region, the isolation region not extending under the channel region; and

source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region.

13. The semiconductor device as recited in Claim 12 wherein the isolation region comprises an oxide.

14. The semiconductor device as recited in Claim 12 wherein the second portion comprises polysilicon.

15. The semiconductor device as recited in Claim 12 wherein the isolation region extends through a transistor tub.

16. The semiconductor device as recited in Claim 12 wherein the source/drain regions are first source/drain regions of a first transistor, and the semiconductor device further includes second source/drain regions of a second adjacent transistor, wherein the first source/drain regions are isolated from the second source/drain regions by the isolation region.

17. A semiconductor device, comprising:

a first transistor located adjacent a second transistor, wherein both the first and second transistors are located over a semiconductor substrate;

an isolation region located between the first and second transistors; and

source/drain regions associated with each of the first and second transistors, each of the source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region.

18. The semiconductor device as recited in Claim 17 wherein the isolation region comprises an oxide.

19. The semiconductor device as recited in Claim 17 wherein the second portion comprises polysilicon.

20. The semiconductor device as recited in Claim 17 wherein the isolation region extends through a transistor tub.

21. A method of manufacturing a semiconductor device, comprising:

providing a semiconductor substrate;

creating a gate above the semiconductor substrate;

forming an isolation region;

forming at least one of a source/drain region above the isolation region.

22. The method as recited in Claim 21 wherein forming an isolation region includes forming an isolation region adjacent to the semiconductor region.

23. The method as recited in Claim 21 wherein forming an isolation region includes forming an isolation region that is not located under a channel region.

24. The method as recited in Claim 21 wherein forming an isolation region includes forming an oxide isolation region.

25. The method as recited in Claim 21 wherein forming the at least one source/drain region includes forming a portion of the at least source/drain region with polysilicon.

26. The method as recited in Claim 21 wherein forming an isolation region includes forming an isolation region that extends through a transistor tub.

27. An integrated circuit, comprising:

semiconductor devices including;

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region;

at least one of a source/drain region formed above the isolation region; and

interconnect structures contacting the semiconductor devices.

28. The integrated circuit as recited in Claim 27 wherein the isolation region is formed adjacent the semiconductor substrate.

29. The integrated circuit as recited in Claim 27 wherein the isolation region is not located under a channel region.

30. The integrated circuit as recited in Claim 27 wherein the isolation region comprises an oxide.

31. The integrated circuit as recited in Claim 27 wherein a portion of the at least one source/drain region comprises polysilicon.

32. The integrated circuit as recited in Claim 27 wherein the

isolation region extends through a transistor tub.

33. The integrated circuit as recited in Claim 27 further including additional active and passive devices.